Latch Placement Technique For Reduced Clock Signal Skew

## ABSTRACT

A method of designing an integrated circuit including executing a placement algorithm to place a set of objects within the integrated circuit. The set of objects includes latched objects and non-latched objects. The algorithm places objects to minimize clock signal delay subject to a constraint on the placement distribution of the latched objects relative to the placement distribution of the non-latched objects. The latched object and non-latched object placement constraints may limit the difference between the latched object center of mass and a non-latched object center of mass. The latched object center of mass equals a sum of size-location products for each latched object divided by the sum of sizes for each latched object. The constraints may require that the latched object center of mass and the non-latched center of mass both equal the center of mass for all objects.